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a memory controller for controlling transfer of data between said memory and said data processor and between said memory and a display, wherein said memory controller comprises:

m-bit terminals, (wherein m is an integer) connected to said memory, for transferring data of m bits successively in a predetermined period of time between said memory and said memory controller,

an n-bit interface, (wherein n is a integer and $n > m$) connected to said data processor, for transferring data of n bits in parallel between said data processor and said memory controller based on an indication from said data processor,

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at least one bit terminal, connected to said display, for transferring serial data between said display and said memory controller,

first converting means for performing conversion between data of plural sets of m bits via said m-bit terminals and data of n bits via said n-bit interface based on an indication from said data processor, and

second converting means for converting said data of plural sets of m bits via said m-bits terminal into said serial data.

14.

58. A graphic processing apparatus comprising:

a memory for storing graphic data;

a data processor for executing a predetermined graphic processing to generate graphic data to be stored in